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10/775,335	02/11/2004	Paul Kimelman	550-519	8558

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EXAMINER	
KAWSAR, ABDULLAH AL	
ART UNIT	PAPER NUMBER
2195	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/775,335	KIMELMAN ET AL.	
	Examiner	Art Unit	
	ABDULLAH AL KAWSAR	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/10/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-26 are pending.

Claim Objections

2. Claims 1-13 are objected to for a potential 101 rejection because of the following informalities: claim 1 is an Apparatus claim without reciting any hardware that performs the steps of claim 1. Applicant is suggested to specify at least one element in claim 1 recited as hardware in specification or amend the claim including a hardware such as "processor" or “memory" .

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-7, 10-12, 14-20 and 23-25 rejected under 35 U.S.C. 103(a) as being unpatentable over Miu et al.(Miu) US Patent No. 4,488,227, in view of Ishimoto et al.(Ishimoto) US Patent No. 5,410,715.

5. As per claim 1, Miu teaches the invention substantially as claim including Apparatus for processing data (col 1, lines 9-12), said apparatus comprising:

processing logic operable to perform processing operations under control of program instructions(col 4, lines 14-19); and

an interrupt controller(col 4, lines 22-24), in response to a first interrupt event, for saving to a stack data store first state data associated with processing being performed when said first interrupt event occurred and for redirecting program instruction execution to a first interrupt handling program (col 4, lines 15-30) and

(i) if said one or more second interrupt events has occurred, then redirecting program instruction execution to a second interrupt handling program without saving(neither pushed nor popped) further state data to said stack data store(abstract lines 10-17 and col 4 lines 36-43); and

(ii) if said one or more second interrupt event has not occurred, then reloading said first state data from said stack data store and to resume said processing that was interrupted by said first interrupt event (col 3 lines 4-12).

6. Miu did not teach detecting one or more higher priority interrupts during the execution of the first interrupt.

7. However, Ishimoto discloses that upon completion of said first interrupt handling program, for detecting if one or more second interrupt events having a higher priority than said processing that was interrupted by said first interrupt event has occurred during execution of said first interrupt handling program (col 4, lines 4-12, lines 16-34).

8. Therefore, it would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of Ishimoto into the method of Miu for detecting one or more higher priority interrupt during the execution of the first interrupt. The modification

would have been obvious because one of the ordinary skills of the art would want to detect the higher priority level interrupts for execution for better interrupt handling and control.

9. As per claim 2, Miu teaches wherein said first state data includes one or more of: a program counter value corresponding a current program execution point (figure 5, sheet 1 element 63, 66, and 64);

a processor status register value corresponding one or more state variables of said apparatus (col 10, lines 14-16); and

one or more data processing register values corresponding to data values held within at least some general purpose data processing registers of said apparatus (col 10, lines 35-55).

10. As per claim 3, Ishimoto teaches wherein said processing being performed when said first interrupt event occurred was one of (col 4 lines 4-14):

execution of an active interrupt handling program, said interrupt controller being a nested interrupt controller permitting a pending interrupt handling program to pre-empt said active interrupt handling program if said active interrupt handling program has a lower priority than said pending interrupt handling program (fig 1,element 1; col 1, lines 31-40; col 7, lines 60-63; col 10 lines 25-28).

Ishimoto does not disclose specifically the processing being the execution of a non-interrupt triggered program.

However, Miu teaches that execution of a non-interrupt triggered program (col 3, lines 60-66).

11. As per claim 4, Ishimoto teaches, wherein said first interrupt event and said one or more second interrupt events each have respective priority values, said interrupt controller being operable to compare said respective priority values to determine if any of said one or second interrupts event has a higher priority than said first interrupt event and if so to pre-empt execution of said first interrupt handling program with execution of said a second interrupt handling program (col 4, lines 65-68; col 5, lines 1-19).

12. As per claim 5, Ishimoto teaches wherein said respective priority values are programmable values (col 4, lines 61-64).

13. As per claim 6, Ishimoto teaches wherein said interrupt controller is responsive to a late interrupt signal during reloading of said first state data to abort a return to said processing being performed when said first interrupt event occurred and instead redirect execution to an interrupt handling program associated with said late interrupt signal (col 9, lines 5-22).

14. As per claim 7, Ishimoto teaches wherein if such a said second interrupt event has occurred, then redirection of program instruction execution to said second interrupt handling program occurs without reloading said first state data from said stack data store (col 9, lines 5-55).

15. As per claim 10, Miu teaches wherein transfer of data values to said stack data store under control of said interrupt controller is performed in parallel with and asynchronously to loading of program counter location and program instructions into an instruction pipeline prior to execution (col 10, lines 35-43).

16. As per claim 11, Miu teaches, wherein said interrupt controller is responsive to execution of a return instruction with a predetermined link address value loaded within a link register to perform a return from interrupt operation (col 2, lines 54-59).

17. As per claim 12, Ishimoto teaches wherein said stack data store is a stack memory (col 7, lines 37-41).

18. As per claims 14-20 and 23-25, they are method claims of claim 1-7 and 10-12 above. Therefore, they are rejected under the same rational as claim 1-7 and 10-12 above.

19. Claims 8, 9, 21 and 22 rejected under 35 U.S.C. 103(a) as being unpatentable over Miu et al.(Miu) US Patent No. 4,488,227, in view of Ishimoto et al.(Ishimoto) US Patent No. 5,410,715, and further in view of McMahan.(McMahan) US Patent No. 5,706,491.

20. As per claim 8, the combined method of Miu and Ishimoto does not specifically disclose repairing to undo any partial return call.

21. However, McMahan teaches wherein upon aborting said return, said stack data store is repaired to undo any alterations made by partial completion of said return (col 3, lines 54-67; col 4, lines 1-20).

22. Therefore, it would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of McMahan into the combined method of Ishimoto and Miu for repairing any unsuccessful return. The modification would have been obvious because one of the ordinary skills of the art would want to repair the unsuccessful return for future execution of unfinished processes.

23. As per claim 9, McMahan teaches wherein said repair includes repairing one or more of stack pointer data and link register data (col 4, lines 4-20).

24. As per claims 21 and 22, they are method claims of claim 8 and 9 above. Therefore, they are rejected under the same rational as claim 8 and 9 above.

25. Claims 13 and 26 rejected under 35 U.S.C. 103(a) as being unpatentable over Miu et al.(Miu) US Patent No. 4,488,227, in view of Ishimoto et al.(Ishimoto) US Patent No. 5,410,715, and further in view of Raasch et al.(Raasch) US Patent No. 5,237,692.

26. As per claim 13, the combined method of Miu and Ishimoto does not specifically disclose of entering a low power mode when no pending interrupt is available.

27. However, Raasch teaches wherein when there are no pending interrupts said apparatus enters a low power mode in which processing is halted awaiting an interrupt event (col 2, lines 63-68; col 3, lines 1-4).

28. Therefore, it would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of Raasch into the combined method of Ishimoto and Miu for entering a low power mode when no interrupt to process. The modification would have been obvious because one of the ordinary skills of the art would want to enter a low power mode to conserve power and system resources.

29. As per claim 26, it is a method claim of claim 13 above. Therefore, it is rejected under the same rational as claim 13 above.

Response to Arguments

30. Applicant's arguments filed 02/14/2008 have been fully considered but they are not persuasive.

31. In the remarks applicant argues:

(1) Ishimoto fails to teach one or more second interrupt events having a higher priority than said processing that were interrupted by said first interrupt event.

32. Examiner respectfully disagree to applicant:

i. as to point (1), applicant supports his argument with mentioning that Ishimoto teaches detecting second interrupt having higher priority of the first interrupt not having higher priority than the processing which was interrupted by the first interrupt event. An interrupt event is serviced when the interrupt event has higher priority than the process that is being processed in the processing logic. Interrupt service that has higher priority than the first interrupt has higher priority than the processing event as the first interrupt has higher priority than the processing event that was interrupted. In a nested interrupt routine there are more than one interrupt event that are being serviced and every single one of those interrupt event has higher priority than the processing event (Ishimoto, col 1, lines 17-40). Claim language is broad and does not specify if the second interrupt was detected after completion of the first interrupt service before or after loading the initial interrupted process for processing. Ishimoto teaches detecting a first interrupt with a priority higher than the processing and detecting multiple other interrupt having priority same or higher priority of the interrupt that was completed or being serviced, which means all the interrupts have higher priority than the interrupted process (col 2, lines 20-32).

Conclusion

33. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

34. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abdullah-Al Kawsar whose telephone number is 571-270-3169. The examiner can normally be reached on 7:30am to 5:00pm, EST.

36. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng Ai T. An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

37. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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